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Non-Destructive Failure Analysis of Power Devices via Time-Domain Reflectometry

Kanuj Sharma[1], Simon Kamm[2], Valentyna Afanasenko[1], Kevin Muñoz Barón[1] and Ingmar Kallfass[1]

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***Abstract*— In power electronic applications, transistors are a vital component. They are, however, susceptible to failures due to degradation of the interconnections and the chip itself. This paper presents a non-destructive approach for failure detection and location in power electronic devices using time-domain reflectometry. The proposed measurement and data generation method is applied to a silicon-carbide power transistor where several characteristics (R, L, C, open, short) and the location of the failure is simulated and characterized. Moreover, the method is also used to find the intrinsic properties of the transistor such as parasitic inductance and capacitance. The data generated is mapped to physical equations, however, the reflected signal of the time-domain reflectometry can be noisy due to multiple discontinuities in the transmission path. Therefore, the simulation and measurement data can be used to train hybrid machine learning models for parameter extraction which automates the failure analysis in Industry4.0 processes to ensure a smart and reliable manufacturing process.**

I. INTRODUCTION

In semiconductor manufacturing and applications, the 100 % success rate of failure analysis (FA) is challenging [1] and it is a big concern in other industrial domains as well. In the field of power electronics, silicon-carbide (SiC) and gallium-nitride (GaN) transistors are relatively new technologies as compared to conventional silicon-based (Si) transistors. They outperform Si transistors in terms of power and switching characteristics. Being relatively new technologies, the manufacturing process of SiC and GaN is complex and has lead to many manufacturing defects because of lattice mismatch and other factors [2]. Hence, failures in the semiconductor are inevitable. However, to make the manufacturing and application process effective and efficient, detection, prediction and location of the possible failure are vital.

Electrical reflectometry is one of the non-destructive methods for failure analysis where a high-frequency signal or pulse is incident (V_{in}) into the device under test (DUT). Because of discontinuities and impedance mismatch, the reflections (V_{m}) are measured. The reflection coefficient ρ is calculated as

$$\rho = \frac{Z_{\mathrm{L}} - Z_0}{Z_{\mathrm{L}} + Z_0} \tag{1}$$

where Z_0 is the characteristic impedance of the transmission and measurement system (50 Ω in this paper), and Z_L is the impedance of the discontinuity (R, L, C). The reflection coefficient for an open and short circuit is 1 and -1 respectively. There are several electrical reflectometry approaches based on the type of incident signal and analysis processes such as Time-Domain Reflectometry (TDR), Time-Frequency Domain Reflectometry (TFDR), Multicarrier Reflectometry (MCR) Frequency Domain Reflectometry (FDR), Binary Time Domain Reflectometry (BTDR), Chaos Time Domain Reflectometry (CTDR), Noise Domain Reflectometry (NDR), Orthogonal Multi-Tone Time Domain Reflectometry (OMTDR), Sequence (STDR) and Spread Spectrum Time Domain Reflectometry (SSTDR) [3]. However, in all of the methods, the measured data is complex and difficult to analyze. Therefore, automated techniques like machine learning models are required for the analysis [3]. In this paper, time-domain reflectometry is used to detect and locate the discontinuity.

In a power electronics system, the electromagnetic interference of the converter has a large impact on the operation. The parasitics of the interconnects also play a vital role ranging from bus-bar interconnects to the device oxide layer. Especially for CMOS technologies, the measurement process is limited in terms of accuracy because of the high level of leakage across the gate

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[1] Institute of Robust Power Semiconductor Systems, University of Stuttgart, Stuttgart, Germany kanuj.sharma@ilh.uni-stuttgart.de

[2] Institute of Automation and Software Systems, University of Stuttgart, Stuttgart, Germany

dielectric. To characterize the parasitics of the interconnects in a switching converter, the TDR offers a high-speed measurement solution with higher accuracy [4], [5], [6]. Ariga et al. [7] present a method to measure the intrinsic capacitance of a MOSFET using TDR by varying the DC bias voltage. Along with parasitic capacitance, the inductance in the electrical path also influences the switching speed and losses significantly. Hence, the TDR can be used to measure the self and mutual inductance more precisely than conventional measurement techniques [8]. Similar TDR techniques to measure parasitic inductance with 2-point and 3-point measurement system is presented in [9]. A SiC power transistor which is a complex RLC circuit is used as the DUT and intrinsic characteristics of the transistor are used as discontinuities.

II. Time-Domain Reflectometry

The employed time-domain reflectometry measurement setup in this paper mainly consists of a fast-rising step generator and high bandwidth voltage measurement devices such as an oscilloscope. The step signal is injected into the DUT and the reflections are measured with the oscilloscope. The amplitude of reflections is defined by the impedance of the DUT. The reflected signal of non-dispersive frequency components (open, short, R) is also a step signal. The location of the discontinuity can be calculated using the formula

$$D = v_{\mathrm{p}} \cdot \frac{t}{2} \tag{2}$$

where D is the distance of the discontinuity from the source of the incident signal, t is the transit time from the oscilloscope to the point of discontinuity and back again, and v_{p} is the propagation velocity in the transmission path.

III. Simulations and Measurements

A. Measurement Concept

The block diagram of the measurement concept is shown in Fig.1. The measurement consists of a step generator, power divider, coaxial cable for the connection, power supply and the DUT. The power divider used in the setup is a three-terminal device with 3 dB power loss in all directions. The fast-rising step signal V_{in} is injected into port 2 of the power divider using a step generator. The reflected signals V_{m} are measured at port 3 of the power divider using an oscilloscope. Since a silicon-carbide power transistor is chosen as the DUT which is an active device, a bias tee is connected between the DUT and port 1 of the power divider in order to bias the gate of the transistor. The bias tee separates the DC and AC components of the bias input which protects the high-frequency measurement instruments from the applied high DC voltage at the gate. Hence, the measurements can be performed in the on-state of the transistor.

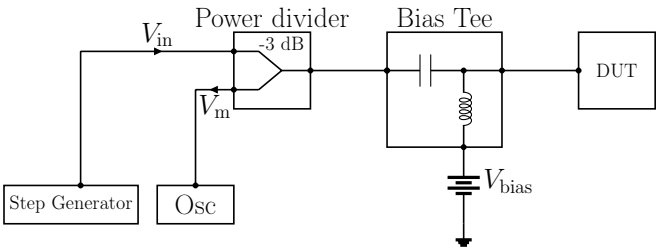

Fig. 1. Block diagram of measurement concept

B. Hard and Soft Failures

To completely understand the measurement setup, hard and soft failures are considered and analyzed in this paper. Hard failures are due to either open or short circuits whereas soft failures are the ones where the impedance (resistive, inductive or capacitive) of the DUT changes. In time-domain reflectometry, when

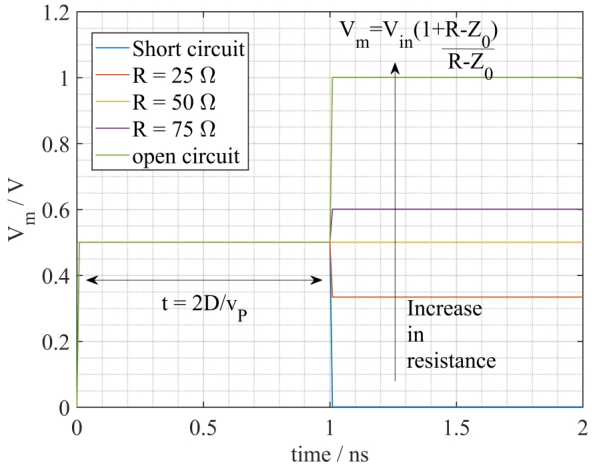

Fig. 2. Time-domain reflectometry at different resistances

there is an open circuit at the DUT, the load impedance Z_{L} approaches infinity and the whole injected signal is reflected. Therefore the calculated reflection coefficient, ρ from eq. (1) is 1. This means at port 3 of the power divider, the measured signal V_{m} is double the input voltage V_{in}. Similarly, for short-circuit failure, the load impedance is 0, therefore, the calculated reflection

coefficient is -1. Simulations for both of the hard failures, open and short circuits, are shown in Fig 2.

Soft failures are considered either as single or the mix of resistive, inductive or capacitive discontinuity. For ($Z_{\mathrm{L}} = Z_0 = 50\ \Omega$), there are no reflections. Therefore, V_{m} stays constant with no discontinuity. The amplitude of V_{m} has the boundary conditions $[0, 2 \cdot V_{\mathrm{in}}]$ and follows the following equation depending on the magnitude of resistive failure:

$$V_{\mathrm{m,R}} = V_{\mathrm{in}} \cdot \left[1 + \frac{R - Z_0}{R + Z_0}\right] \tag{3}$$

For the simulated cases, one resistive discontinuity $R = 75\ \Omega$ is higher than the characteristic impedance and another $R = 25\ \Omega$ is less than the characteristic impedance. The calculated reflection coefficients are 1/5 and -1/3 respectively, shown in Fig. 2.

If there is a capacitive discontinuity along with the resistive discontinuity in series, the formula for V_{m} employs the complex impedance. The capacitor follows the law of conservation of charge, the voltage across a capacitor cannot be changed instantaneously but has a time constant τ and follows the following equation

$$i_{\mathrm{c}}(t) = C \cdot \frac{dv_{\mathrm{c}}(t)}{dt} \tag{4}$$

where i_{c} and v_{c} are the current and voltage across the capacitor. After applying the input voltage, when time t tends to infinity, the capacitor is fully charged and reaches the steady state. Therefore, equation (4) can be written as

$$\lim_{t \to +\infty} i_{\mathrm{c}}(t) = C \cdot \frac{dv_{\mathrm{c}}(\infty)}{dt} = 0 \tag{5}$$

The steady-state value of i_{c} equals 0 because of no change in the voltage across the capacitor with time t tends to infinity. Hence, the capacitor acts as an open circuit.

Using Laplace transformation with initial conditions, the equation (3) will become

$$V_{\mathrm{m,RC}} = V_{\mathrm{in}} \cdot \left[2 - \left(1 + \frac{R - Z_0}{R + Z_0}\right) \cdot e^{\frac{-t}{\tau_{\mathrm{RC}}}}\right] \tag{6}$$

because the capacitance has the characteristic impedance and the resistive failure in series, the time constant τ_{RC} is

$$\tau_{\mathrm{RC}} = (R + Z_0) \cdot C \tag{7}$$

The simulations are performed for R = 75 Ω and different capacitor values from 2 to 10 pF with 2 pF steps and shown in Fig. 3. The time constant τ increases with the increase in capacitance. Nevertheless, the V_{m} approaches $2 \cdot V_{\mathrm{in}}$ as t tends to infinity referring to open-circuit conditions.

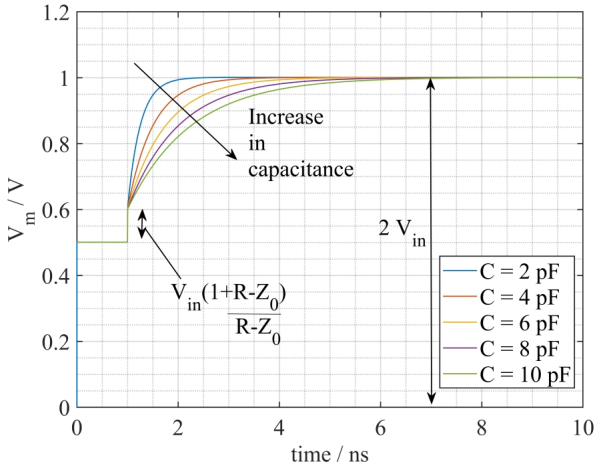

Fig. 3. Time-domain reflectometry for different capacitance at $R = 75\ \Omega$

Similarly, if there is an inductive and resistive discontinuity together in series, there is also a time constant associated. An inductor follows the law conservation of flux ϕ, hence, the current flowing through the inductor cannot be changed instantaneously. Initially, there is no current flowing through the inductor, i.e. at $t = 0$, $i_{\mathrm{L}} = 0$ corresponds to the open circuit condition. The voltage drop across the inductor is

$$v_{\mathrm{L}}(t) = L \cdot \frac{di_{\mathrm{L}}(t)}{dt} \tag{8}$$

where i_{L} and v_{L} are the current and voltage across the inductor. After applying the input voltage, at t tends to infinity, the inductor is fully energised and reaches the steady-state. The equation for the voltage drop across the inductor (8) can be written as

$$\lim_{t \to +\infty} V_{\mathrm{L}}(t) = L \cdot \frac{di_{\mathrm{L}}(\infty)}{dt} = 0 \tag{9}$$

The steady-state value of V_{L} is equal to 0 because of no voltage drop across the inductor with time t approaches infinity. Hence, the inductor acts as a short circuit. Again using Laplace transformation, the equation (3) becomes

$$\mathrm{V_{m,RL}} = V_{\mathrm{in}} \cdot \left[\left(1 + \tfrac{R - Z_0}{R + Z_0}\right) + \left(1 - \tfrac{R - Z_0}{R + Z_0}\right) \cdot e^{\frac{-t}{\tau_{\mathrm{RL}}}}\right] \tag{10}$$

The inductor has characteristic impedance and the resistive discontinuity in series, the time constant τ_{RL}

can be defined as

$$\tau_{\mathrm{RL}} = \frac{L}{R + Z_0} \tag{11}$$

The simulations are performed and shown in Fig. 4. R is kept constant at 25 Ω and inductance is varied from 2 to 8 nH with 2 nH steps. Since there is no voltage drop across the inductor at $t \to \infty$, the V_{m} saturates at $V_{\mathrm{m,R}}$ ($V_{\mathrm{m,L}} = V_{\mathrm{m,R}}$).

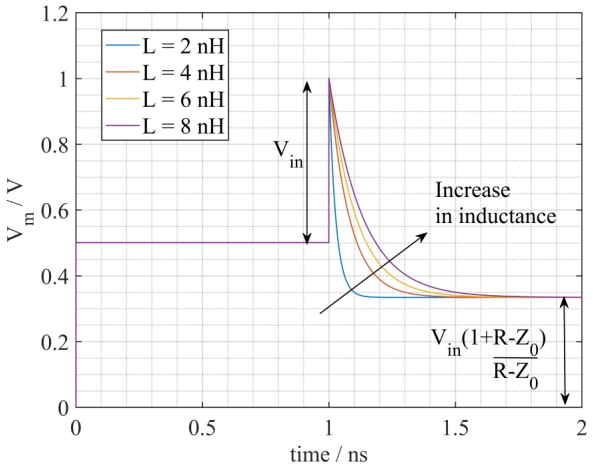

Fig. 4. Time-domain reflectometry for different inductance at $R = 25\ \Omega$

The TDR measurements are performed at the gate-source terminal of the SiC power transistor SCT2160KE from ROHM using the proposed method and presented in Fig. 5. The gate-bias voltage is varied from -8 V to 6 V in 2 V steps. The drain terminal voltage is kept at 0 V. It is observed that the time constant decreases when the gate-bias voltage V_{bias} increases from -8 V to -2 V. The constant of the TDR measurement increases again when gate-bias voltage is further increased from 2 V to 6 V. When the gate-bias voltage is between -2 V to 2 V, the time constant remains comparatively less and constant. To verify this behaviour, gate-source capacitance is measured at different gate-bias voltage, shown in Fig 6.

The capacitive behaviour in TDR compliments both, the TDR measurements on SiC (Fig. 5) and simulations (Fig. 3), where the time constant of the curves at different V_{bias} before saturation at $2 \cdot V_{\mathrm{m}}$ increases with the increase in capacitance magnitude.

C. Calibration

The accuracy and precision of the time-domain reflectometry are vital otherwise it can lead to false information. The bandwidth, electrical noise and blind spots,

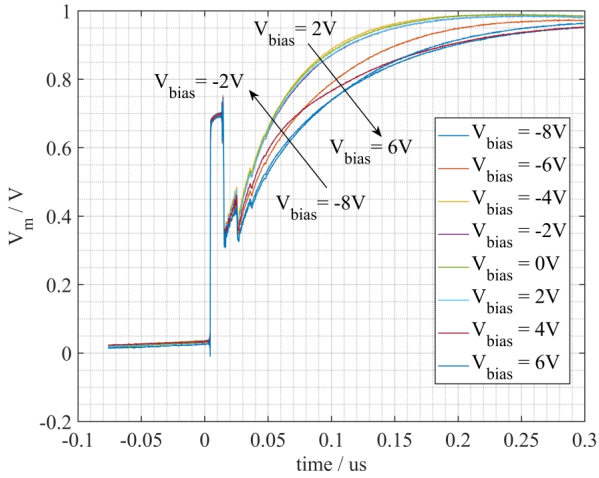

Fig. 5. Time-domain reflectometry measurement for SiC transistor

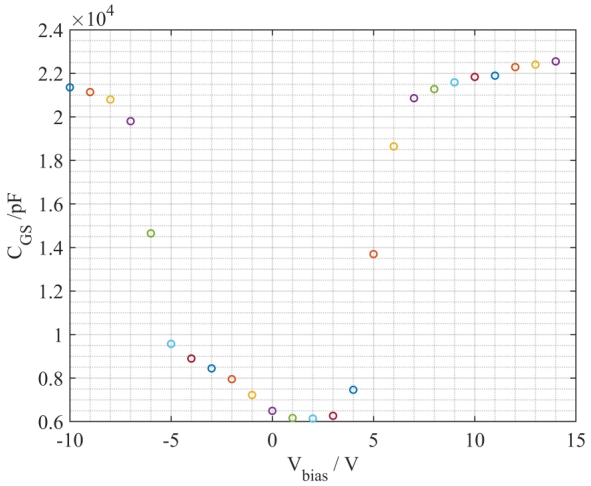

Fig. 6. Gate-source capacitance vs. gate-bias voltage

etc. defines how accurately the fault is detected and located [3]. One of the considerations is the bandwidth of the measurement setup. Larger bandwidth results in higher accuracy in terms of spatial resolution of the measurement data. The bandwidth requirement of the system is defined by the rise time of the injected step signal

$$\mathrm{Bandwidth} = \frac{0.35}{t_{\mathrm{r}}} \tag{12}$$

where t_{r} is the rise time of the step input to the system. The measurement at different rise times is shown in Fig. 7. The rise time is varied from 0 to 100 ps with a log scale. The accuracy of the reflectometry is higher with lower rise time.

Electrical noise in the system should be taken into

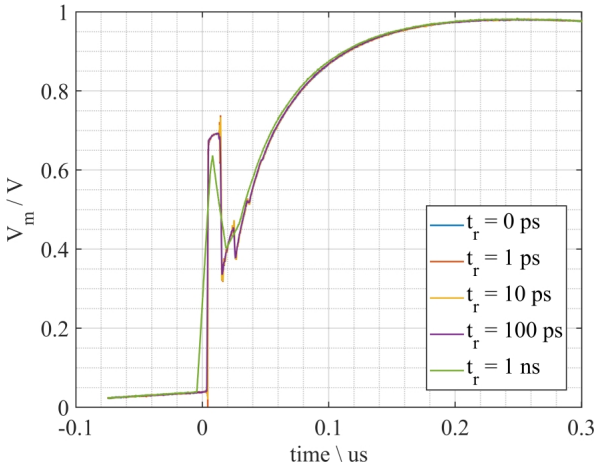

Fig. 7. Time domain reflectometry for SiC with different rise time

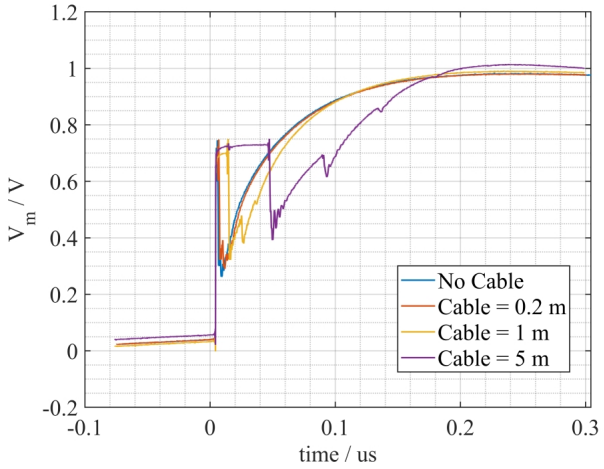

Fig. 8. Time-domain reflectometry with different cable length

account while performing time-domain reflectometry with the proposed method. The measurement data may vary with an unintentional impedance variation e.g. transmission line impedance can vary while connecting and reconnecting the cables. While performing reflectometry, the movement of connected cables can create mechanical vibrations which affects the measurement results. Moreover, the change in ambient environmental conditions like temperature, humidity, etc can also limit the practical time-domain reflectometry application. Another parameter that should be considered is 'blind spots'. Normally, the blind spots are at the start of the cable [3]. When the fast-rising step signal is injected into the DUT, there is large reflections and noise. If the failure of the DUT is close to the injection point, the reflected fault diagnose signal is superimposed with the noise. This superimposed measured signal is difficult to analyse. To show these effects, the measurements are performed at different cable lengths between power divider and bias tee, shown in Fig 8.

All the above-mentioned parameters can be de-embedded from the measurement result with simple calibration. Baselining can be used to remove these ambiguities from the system where the TDR signatures at normal conditions are subtracted from the actual TDR measurements. Prior knowledge of the system without DUT connected is required for this post-measurement task. Therefore, the measurements are performed for short, open and 50 Ω at the DUT port. The measurements are shown in Fig. 9. The multiple reflections can be seen because of the several connectors and cables in the measurement system. Each connector-cable junction creates a complex overlapping reflection. Especially while analysing soft failures, each additional reflection reduces the amplitude of V_{m}, hence, the dynamical range is reduced. This leads to non-detection of the soft failures or possible inaccurate measurement. The artificial intelligence approaches such as neural network [10], iterative evaluation of network [11], teaching-learning optimization [12], genetic algorithms [10], particle swarm optimization [13], backtracking search optimization [14], etc. can be used to de-embed the effect of the measurement circuit.

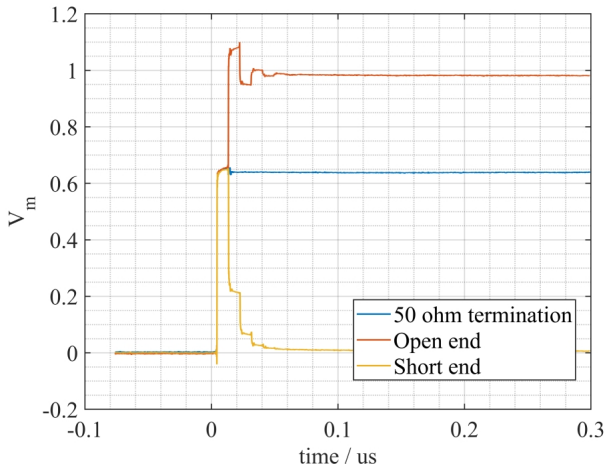

Fig. 9. Calibration: Short, open and DUT at the DUT terminal

IV. CONCLUSION

A time-domain analysis technique is simulated and implemented on a silicon carbide power transistor. The time-domain analysis can be used to determine the behaviour of the discontinuity (R, L, C), the intrinsic

characteristics of the transistor can also be calculated. Using the proposed method, the data can be generated which can be used for further complex analysis using machine learning models for failure or discontinuity analysis. Since the generated data is motivated by physics-based equations, machine learning hybrid models can be implemented. In time-domain reflectometry, different considerations are explained and taken into account for generating an accurate and precise database.

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